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# Design and Analysis of a Low-Power High-Frequency CMOS Low-Pass-Filter-Based Current-Mirror Sinusoidal Quadrature Oscillator

# การออกแบบและวิเคราะห์วงจรออสซิลเลเตอร์รูปคลื่นซายน์แบบครอดราเจอร์เทคโนโลยี CMOS กำลังไฟฟ้าต่ำ ย่านความถี่สูง โดยใช้วงจรกรองผ่านความถี่ต่ำแบบวงจรสะท้อนกระแส

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## บทคัดย่อ

การออกแบบและวิเคราะห์วงจรออสซิลเลเตอร์รูปคลื่นซายน์แบบครอดราเจอร์เทคโนโลยี CMOS กำลังไฟฟ้าต่ำ ย่านความถี่สูง นำเสนอโดยการใช้วงจรกรองผ่านความถี่ต่ำแบบวงจรสะท้อนกระแส 2$^{nd}$-order, วงจรกรองผ่านความถี่ต่ำแบบวงจรสะท้อนกระแส 1$^{st}$-order และ วงจร bilinear transfer function แบบวงจรสะท้อนกระแส ซึ่งมีเทคนิคบนพื้นฐาน 2 แบบดังนี้ แบบที่ 1 ค่าคงที่ของเวลา (time constant) ซึ่งเกิดขึ้นภายในวงจรสะท้อนกระแส คือ ค่าของตัวเก็บประจุภายในและค่าความนำ (transconductance) ของทรานซิสเตอร์แบบ NMOS และแบบที่ 2 คือ ค่าความต้านทานแบบลบ RN มาจากภาระทางไฟฟ้าที่เป็นความต้านทาน (load resistor RL) ของวงจรสะท้อนกระแส และ ในตัววงจรก็ไม่มีการใช้ตัวเก็บประจุและตัวเหนี่ยวนำที่ต่อมาจากภายนอกวงจร

ซึ่งแสดงผลดังนี้ ความถี่สูงสุดของการกำเนิดสัญญาณของวงจร คือ 1.9 GHz และสามารถเปลี่ยนช่วงความถี่ได้ในการกำเนิดสัญญาณได้ 370 MHz หรือ 21.6%, กำลังไฟฟ้าประมาณ 0.45 mW, ค่า amplitude matching มีค่าที่ดีกว่า 0.05 dB, ค่า quadrature phase matching มีค่าที่ดีกว่า 0.15 degrees, ค่าความผิดเพี้ยนฮาร์มอนิครวม (THD) มีค่าน้อยกว่า 0.3%, ค่า carrier to noise ratio (CNR) มีค่า 90.01 dBc/Hz ที่ 2 MHz วัดจากความถี่ที่กำเนิดสัญญาณ, ค่า figures of merit เรียกว่า normalized carrier-to-noise ratio ($CNR_{norm}$) มีค่า 153.03 dBc/Hz ที่ 2 MHz วัดจากความถี่ที่กำเนิดสัญญาณ, ค่าอัตราส่วน (ratio) ระหว่างความถี่ของการกำเนิดสัญญาณ ($f_0$) ต่อความถี่ที่มีอัตราการขยายเป็นหนึ่งของทรานซิสเตอร์ ($f_T$) คือ 0.25, ความถี่การกำเนิดสัญญาณของวงจรมีการเปลี่ยนช่วงความถี่ระหว่าง 1.8 GHz ถึง 1.9 GHz เมื่อค่าของอุปกรณ์ภายในวงจรมีการปลี่ยนแปลงระหว่าง -1.5% ถึง 1.5% ขณะที่ความถี่การกำเนิดสัญญาณของวงจรมีการเปลี่ยนช่วงความถี่ระหว่าง 1.9 GHz ถึง 1.7 GHz เมื่อค่าของอุณหภูมิภายในวงจรมีการปลี่ยนแปลงระหว่าง 20 °C และ 100 °C และได้แสดงผลการเปรียบเทียบกับเทคนิคอื่นๆ ที่เกี่ยวข้องด้วย

**คำสำคัญ:** กำลังไฟฟ้าต่ำ ย่านความถี่สูง วงจรออสซิลเลเตอร์รูปคลื่นซายน์แบบครอดราเจอร์ วงจรกรองผ่านความถี่ต่ำแบบวงจรสะท้อนกระแส วงจรสะท้อนกระแส ความต้านทานแบบลบ

## Abstract

The design and analysis of a low-power high-frequency CMOS sinusoidal quadrature oscillator is presented through the use of two $2^{nd}$-order low-pass current-mirror (CM)-based filters, a $1^{st}$-order CM low-pass filter and a CM bilinear transfer function. The technique is relatively simple based on (i) inherent time constants of current mirrors, i.e. the internal capacitances and the transconductance of a diode-connected NMOS, and (ii) a simple negative resistance $R_N$ formed by a load resistor $R_L$ of a current mirror. Neither external capacitances nor inductances are required. The oscillation frequency ($f_0$) is 1.9 GHz and is current-tunable over a range of 370 MHz or 21.6%. The power consumption is at approximately 0.45 mW. The amplitude matching and the quadrature phase matching are better than 0.05 dB and 0.15°, respectively. Total harmonic distortions (THD) are less than 0.3%. At 2 MHz offset from the 1.9 GHz, the carrier to noise ratio (CNR) is 90.01 dBc/Hz, whilst the figure of merit called a normalized carrier-to-noise ratio ($CNR_{norm}$) is 153.03 dBc/Hz. The ratio of the oscillation frequency ($f_0$) to the unity-gain frequency ($f_T$) of a transistor is 0.25. The variations of components between -1.5% and 1.5% indicates that the oscillation frequency is varied in the range between 1.8 GHz to 1.9 GHz, whilst the variations of temperature between 20 °C and 100 °C indicates that the oscillation frequency is downed from 1.9 GHz to 1.7 GHz. Comparisons to other approaches are also included.

**Keywords:** Low-Power, High-Frequency, Sinusoidal Quadrature Oscillator, Low-Pass Current-Mirror-Based Filter, Current-Mirror, Negative Resistance

## I. Introduction

Quadrature oscillators (QOs) typically provide two sinusoids with 90° phase difference for a variety of applications such as in receivers for wireless communication systems (GSM, PCS or Bluetooth, etc.). For example, GSM 1800-MHz or PCS 1.9-GHz receivers require operating frequencies between 1.805 to 1.99 GHz (Fenk, 1997). QOs are important for receivers and examples of reasons are as follows:

a) Hartley and Weaver image-reject receivers (Razavi, 1997a), superheterodyne receivers (Parssinen, 2001), zero-intermediate frequency (zero-IF) or direct-conversion receivers (Gatta, et al., 2004), low-IF (Hughes, et al., 2002), digital IF (Parssinen, 2001) receivers and direct digital or digital RF receivers (Parssinen, 2001) all employ the quadrature downconverter.

b) Double low-IF and wide-band IF receivers (Parssinen, 2001) employ the double quadrature downconverter.

Generally, QOs can be either non-linear or linear types. Non-linear QOs such as relaxation and ring QOs are usually realized using periodically switching mechanisms and therefore outputs may not be readily low-distortion sinusoids (Johns and Martin, 1997). In contrast, linear QOs employ frequency-selective networks such as RC or LC circuits and consequently low-distortion sinusoids can be readily generated (Sedra and Smith, 1998).

As mentioned earlier, the required operating frequencies between 1.805 to 1.99 GHz in the receivers are typically utilized in the GSM 1800 MHz or PCS 1.9 GHz (Fenk, 1997). In the well publicized literature, no other linear (sinusoidal) QOs using RC techniques have been reported for tuning ranges of high oscillation frequencies from 1.805 to 1.99 GHz. Existing RC techniques for QOs include all-pass filters (Banlue Srisuchinwong, 2000), operational transconductance amplifiers using capacitors (OTA-C) (Kiattisak Kumwachara and Wanlop Surakampontorn, 2003), operational transresistance amplifiers (OTRA) (Cakir, Cam, and Cicekoglu, 2005), current conveyers (Horng, Chou, and Shiu, 2006) and negative resistance (Sedra and Smith, 1998). Such RC techniques have suffered not only from relatively low oscillation frequencies between 40 kHz to 8 MHz due to the use of relatively large off-chip capacitors, but also from relatively high power consumptions. However, an existing RC linear QO has exploited techniques using internal capacitances of BJTs (Sitthichai Pookaiyaudom and Jirayuth Mahattanakul, 1995) for a high oscillation frequency, but the oscillation frequency is still a relatively low oscillation at 0.58 GHz.

Alternative LC techniques using CMOS (Andreani, 2002; Kao and Wu, 2000; Razavi, 1997b) offer high oscillation frequencies between 1.8 to 1.97 GHz, whilst their power consumption is relatively high; between 15 to 50 mW. Recently, non-linear QOs have exploited techniques using internal capacitances of either MOS (Anand and Razavi, 2001; Bautista and Aranda, 2004) or BJTs (Finocchiaro, et al., 1999; Van Der Tang and Kasperkovitz, 1997) for a high oscillation frequency between 1.8 to 2.5 GHz. However, the ratios of the oscillation frequency ($f_0$) to the unity-gain frequency ($f_T$) (Sedra and Smith, 1998) of a transistor are in the region of 0.1 to 0.2, while the power consumption is relatively high between 7.01 to 100 mW.

Surveys of existing RC linear QOs using techniques of BJT current mirrors have been reported in (Sitthichai Pookaiyaudom and Kanok Samootrut, 1987) and (Sitthichai Pookaiyaudom and Rungsimant Sitdhikorn, 1996). Such CM oscillators have been for non-quadrature oscillators, but may be, although not explicitly indicated, modified for QOs. However, they have suffered not only from relatively low oscillation frequencies between 1 MHz to 580 MHz, but also from relatively high power consumption; between 105 mW to 297 mW. Recently, existing RC linear QOs exploited techniques using both internal capacitances of MOS and MOS current mirrors (Adisorn Leelasantitham and Banlue Srisuchinwong, 2003, 2004a, 2004b, 2004c, 2008) have been demonstrated for high oscillation frequencies such as 1.01 GHz, 2.46 GHz, 2.83 GHz and 3.02 GHz, but the oscillation frequencies are not tuned in the range from 1.805 to 1.99 GHz. Therefore, current mirrors are one of the most basic building blocks for current sources or current sinks in the design of low-cost low-power integrated circuits where the basic concepts of current mirrors have been well described in many textbooks, such as in (Sedra and Smith, 1998).

In this paper, design and analysis of a low-power high-frequency CMOS sinusoidal quadrature oscillator is presented through the use of two 2$^{nd}$-order low-pass current-mirror (CM)-based filters, a 1st-order CM low-pass filter and a CM bilinear transfer function. The technique is relatively simple based on (i) inherent time constants of current mirrors, i.e. the internal capacitances and the transconductance of a diode-connected NMOS, and (ii) a simple negative resistance $R_N$ formed by a load resistor $R_L$ of a current mirror. Neither external capacitances nor inductances are required. The oscillation frequency ($f_0$) is 1.9 GHz and is current-tunable over a range of 370 MHz or 21.6%. The power consumption is at approximately 0.45 mW. The amplitude matching and the quadrature phase matching are better than 0.05 dB and 0.15°, respectively. Total harmonic distortions (THD) are less than 0.3%. At 2 MHz offset from the 1.9 GHz, the carrier to noise ratio (CNR) is 90.01 dBc/H, whilst the figure of merit called a normalized carrier-to-noise ratio ($CNR_{norm}$) is 153.03 dBc/Hz. The ratio of the oscillation frequency ($f_0$) to the unity-gain frequency ($f_T$) of a transistor is 0.25. The variations of components between -1.5% and 1.5% indicates that the oscillation frequency is varied in the range between 1.8 GHz to 1.9 GHz, whilst the variations in temperature between 20 °C and 100 °C indicates that the oscillation frequency is downed from 1.9 GHz to 1.7 GHz. Comparisons to other approaches are also included.

## II. Designed and Proposed Techniques

### A. Circuit Descriptions

Figures 1 and 2 show the small-signal block diagrams and the circuit configuration, respectively, of the 1.9-GHz, 0.45-mW 2-V CMOS low-pass-filter-based current-mirror sinusoidal quadrature oscillator (Adisorn Leelasantitham and Banlue Srisuchinwong, 2007). As shown in Fig. 1, the circuit for the low-pass-filter-based technique consists of four simple cascaded current-mirror (CM) filters connected together in a closed loop as follows:

(a) a 2nd-order low-pass CM-based filter $F_1$ consists of
- (a.1) a 1st-order CM low-pass filter (LPF) $F'_1$ formed by a current mirror ($Q_1$, $Q_2$),
- (a.2) a 1st-order CM low-pass filter (LPF) $F'_2$ formed by a current mirror ($Q_3$, $Q_4$),

(b) a 2nd-order low-pass CM-based filter $F_2$ consists of
- (b.1) a 1st-order CM low-pass filter (LPF) $F'_3$ formed by a current mirror ($Q_5$, $Q_6$),
- (b.2) a 1st-order CM low-pass filter (LPF) $F'_4$ formed by a current mirror ($Q_7$, $Q_8$),

(c) a 1st-order CM low-pass filter (LPF) $F_3$ formed by a current mirror ($Q_9$, $Q_{10}$),

(d) a CM bilinear transfer function (BLT) $F_4$ described in terms of a negative resistance ($R_N$ = $-R_L$) where $R_L$ is a resistor load of a current mirror ($Q_9$, $Q_{10}$).

In terms of DC analysis, PMOS transistors $Q_{11}$ to $Q_{18}$ and a resistor $R_1$ form sets of DC current mirrors ($Q_{11}$ to $Q_{18}$, $R_1$) for the current-steering circuits, and therefore provide DC currents I, 2I or $G_0I$ for $F_1$, $F_2$ or $F_3$, where $G_0$ is an appropriate gain factor. A resistor $R_L$ provides a DC current $G_0I$ to the output of $F_3$, where $G_0$ is an appropriate gain factor.

In terms of small-signal (SS) analysis, the four CM filters $F_1$, $F_2$, $F_3$ and $F_4$ can be described in terms of current gains $F_1(s)$, $F_2(s)$, $F_3(s)$ and $F_4(s)$, respectively, where the physical frequencies s = jω. Firstly, the current gain $F_1(s) = i_{O1} / i_{in}$, where $i_{in}$ and $i_{O1}$ are input and output small-signal currents of $F_1$ at nodes N and S, respectively. Secondly, the current gain $F_2(s) = i_{O2} / i_{O1}$, where $i_{O1}$ and $i_{O2}$ are input and output SS currents of $F_2$ at nodes N′ and S′, respectively. Thirdly, the current gain $F_3(s) = i_{O3} / i_{O2}$, where $i_{O2}$ and $i_{O3}$ are input and output SS currents of $F_3$ at nodes T and U, respectively. Finally, as will be seen later in Section IID, the current gain $F_4(s) = i_{in} / i_{O3}$ of filter $F_4$ is a bilinear transfer function, where $i_{O3}$ and $i_{in}$ are input and output SS currents of $F_4$ at node N. It can be seen from Fig. 2 that the circuits are all simple current mirrors.

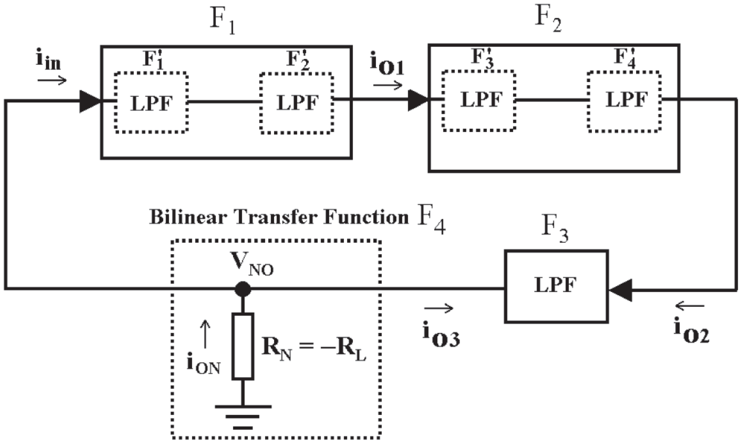


**Fig. 1** Small-signal block diagrams of the 1.9-GHz, 0.45-mW, 2-V CMOS low-pass-filter-based current-mirror sinusoidal quadrature oscillator

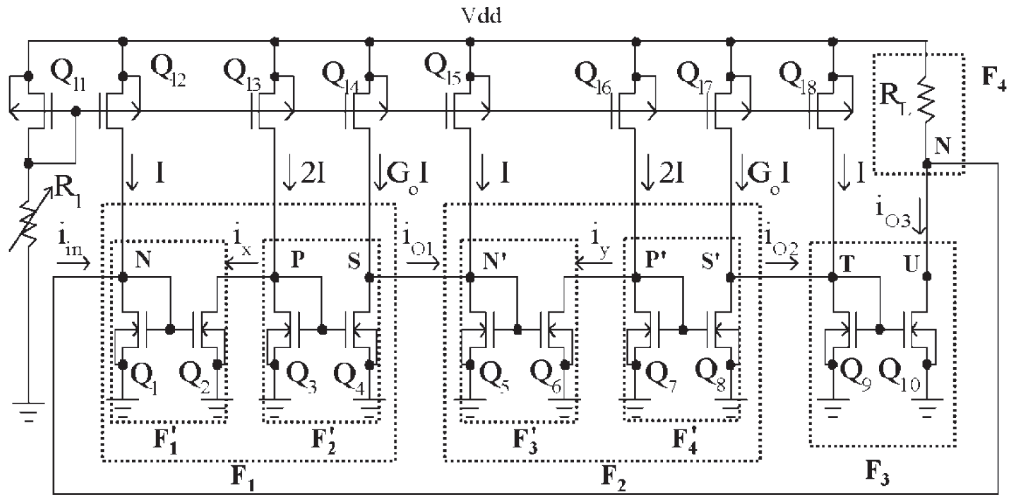


**Fig. 2** Circuit diagrams of the 1.9-GHz, 0.45-mW, 2-V CMOS low-pass-filter-based current-mirror sinusoidal quadrature oscillator

**B. Current-Mirror Filters $F_1$, $F_2$ and $F_3$**

With reference to Fig. 2, let the effect of channel-length modulation of a transistor be negligible. A transconductance $g_{mi}$ of a MOS transistor $Q_i$ for i = 1 to 10 is equal to $g_{mi} = 2I_0/(V_{GSi}-V_T)$, where $V_{GSi}$ is the gate source voltage of $Q_i$, $V_T$ is the threshold voltage and $I_0$ is the bias current of $Q_i$. Table 1 summarizes the small-signal analysis of the three CM filters $F_1$, $F_2$ and $F_3$ in terms of the small-signal currents $i_x$, $i_y$, the output currents $i_{O1}$, $i_{O2}$, $i_{O3}$, the resulting current gains $F_1(s)$, $F_2(s)$, $F_3(s)$ and the internal time constants $\tau_a = C_a / g_{m1}$, $\tau_b = C_b / g_{m3}$, $\tau'_a = C'_a / g_{m5}$, $\tau'_b = C'_b / g_{m7}$ and $\tau_c = C_c / g_{m9}$, where $C_a$, $C_b$, $C'_a$, $C'_b$ and $C_c$ are the total internal capacitances at nodes N, P, N′, P′ and T, respectively, of individual current mirrors. In this technique, details of capacitances $C_a$, $C_b$, $C'_a$, $C'_b$ and $C_c$ will be described further in Section IIIA, whilst details of time constants $\tau_a$, $\tau_b$, $\tau'_a$, $\tau'_b$ and $\tau_c$ will be described further in Section IIIB.

**Table 1** Current gains of the three current-mirror (CM) filters $F_1$, $F_2$ and $F_3$ of Fig. 2.

| Filters | Related Currents | Output Currents | Current Gains |
|---|---|---|---|
| $F_1$ | $i_x = \frac{i_{in}}{(1+s\tau_a)}$ | $i_{O1} = \frac{G_o i_x}{(1+s\tau_b)}$ | $F_1(s) = \frac{i_{O1}}{i_{in}} = \frac{G_0}{(1+s\tau_a)(1+s\tau_b)}$ |
| $F_2$ | $i_y = \frac{i_{O1}}{(1+s\tau'_a)}$ | $i_{O2} = \frac{G_o i_y}{(1+s\tau'_b)}$ | $F_2(s) = \frac{i_{O2}}{i_{O1}} = \frac{G_0}{(1+s\tau'_a)(1+s\tau'_b)}$ |
| $F_3$ | - | $i_{O3} = \frac{G_0 i_{O2}}{(1+s\tau_c)}$ | $F_3(s) = \frac{i_{O3}}{i_{O2}} = \frac{G_0}{(1+s\tau_c)}$ |

### C. Current-Mirror Negative Resistance $R_N$

By setting $F(s) = F_1(s) \cdot F_2(s) \cdot F_3(s)$, it follows from Table I that

$$\frac{i_{in}}{i_{O3}} = \frac{1}{F(s)} \tag{1}$$

The input current $i_{in}$ to filter $F_1$ is equal to

$$i_{in} = \frac{v'_{N0}}{Z_{in}} \tag{2}$$

$$Z_{in} = \frac{1/g_{m1}}{(1+s\tau_a)} \tag{3}$$

where $Z_{in}$ is the input impedance of filter $F_1$ at node N seen by $i_{in}$, $v'_{NO}$ is the small-signal voltage across $Z_{in}$ at node N with respect to node O and node O is the small-signal ground. On the one hand, let $i'_{NO}$ be $i_{O3} + i_{in}$ where $i'_{NO}$ enters node N passing through an impedance $Z_1$ and then leaves node O. The impedance $Z_1$ can be found from (1), (2), (3) and $i'_{NO}$ as shown in (4).

$$\frac{v'_{NO}}{i'_{NO}} = \frac{Z_{in}}{1+F(s)} = Z_1 \tag{4}$$

On the other hand, let $i_{NO}$ be a small-signal current that enters node N passing through $R_L$ and then leaves node O. As $R_L$ is a positive resistance, it follows that

$$\frac{v_{NO}}{i_{NO}} = R_L \tag{5}$$

where $v_{NO}$ is the small-signal voltage across $R_L$ at node N with respect to node O. As $i_{NO} = -i_{ON}$, therefore, $R_L = -v_{NO} / i_{ON}$. Both (4) and (5) follow the passive sign convention and therefore $v'_{NO}$ is positive when $i'_{NO}$ is passing through $Z_1$ and $v_{NO}$ is negative when $i_{ON}$ is passing through $R_L$. The Kirchhoff's current law at node N yields $i'_{NO} - i_{ON} = 0$ and therefore $i'_{NO}$ in (4) can be substituted with $i_{ON}$. The Kirchhoff's voltage law around the loop that consists of $Z_1$ and $R_L$ between nodes N and O yields $-v'_{NO} - v_{NO} = 0$ and therefore $v'_{NO}$ of (4) can be substituted with $-v_{NO}$. It follows from (4) that $v'_{NO} / i'_{NO} = -v_{NO} / i_{ON} = v_{NO} / i_{NO}$. As a result, (4) = (5) and therefore $R_L = Z_{in} / [1 + F(s)]$. Consequently, $i_{in} / i_{O3} = 1 / F(s) = F_4(s)$, where

$$F_4(s) = \frac{-R_N}{(R_N + Z_{in})} \quad (6)$$

$$R_N = -R_L \quad (7)$$

Equation (7) describes a negative resistance $R_N = -(v_{NO} / i_{NO}) = (v_{NO} / i_{ON})$ between nodes N and O, as shown in Fig. 1. It can be seen from (7) that $R_N$ is a simple negative resistance based on an existing resistor $R_L$ of the current mirror ($Q_{11}$, $Q_{12}$, $R_L$).

### D. Current-Mirror Bilinear Transfer Function $F_4$ Using Negative Resistance $R_N$

Equation (6) describes the current gain $F_4(s) = i_{in} / i_{O3}$ of filter $F_4$ in terms of the negative resistance $R_N$. Substituting $Z_{in}$ in (6) with (3) yields

$$F_4(s) = -F_5(s) \quad (8)$$

$$F_5(s) = \frac{A_0(1+s\tau_a)}{(1+s\tau_d)} \quad (9)$$

$$A_0 = \frac{g_{m1}R_N}{(1+g_{m1}R_N)} \quad (10)$$

where $\tau_d = A_0\tau_a$. It can be seen from (8), (9) and (10) that $F_4(s)$ is a CM bilinear transfer function.

### E. Proposed Low-Pass-Filter-Based Current-Mirror Sinusoidal Quadrature Oscillation

It follows from Figs. 1 and 2 that a loop gain $L(s) = F_1(s) \cdot F_2(s) \cdot F_3(s) \cdot F_4(s)$, where $F_1(s)$, $F_2(s)$, $F_3(s)$ are described in Table I and $F_4(s)$ is described in (8) and (9). Therefore $L(s) = -[(G_0)^3(A_0)(1+s\tau_a)]/[(1+s\tau_a)(1+s\tau_b)(1+s\tau'_a)(1+s\tau'_b)(1+s\tau_c)(1+s\tau_d)]$. As will be seen later in Section IIIB, $\tau_b = \tau'_b$, and therefore

$$L(s) = -\frac{(G_0)^3(A_0)}{(1+s\tau_b)^2(1+s\tau'_a)(1+s\tau_c)(1+s\tau_d)} \quad (11)$$

For a sinusoidal oscillation to be sustained at the angular oscillation frequency $\omega_0$, the magnitude $|L(s)|$ and the phase angle $\angle L(s)$ of the loop gain L(s) are equal to unity and zero, respectively. Upon substituting s in (11) with $j\omega_0$ and setting $|L(s)|=1$, the required value of $G_0$ to sustain steady-state sinusoidal oscillations is therefore equal to

$$G_0 = \sqrt[3]{\frac{(1+\omega_0^2\tau_b^2)^2(1+\omega_0^2\tau_a'^2)(1+\omega_0^2\tau_c^2)(1+\omega_0^2\tau_d^2)}{A_0}} \quad (12)$$

Upon setting $\angle L(s) = 0^\circ$ or $-360^\circ$, it follows that $\angle F_1(s) + \angle F_2(s) + \angle F_3(s) + \angle F_5(s) + 180^\circ = 0^\circ$, where a symbol '$\angle x$' indicates a phase angle of x. Setting $\varnothing_a = \angle F_5(s) + \angle F_1(s)$ and setting $\varnothing_b = \angle F_2(s) + \angle F_3(s)$ yield a quadrature oscillation if

$$\varnothing_a = \varnothing_b = -90^\circ \quad (13)$$

On the one hand, it follows from (13) that $\varnothing_a = \angle F_1(s) + \angle F_5(s) = -90^o$ (i.e. $F_1(s) F_5(s) = i_{O1} / i_{O3}$ provides a quadrature phase shift of $\varnothing_a = -(\theta_{O1} - \theta_{O3}) = -90$ degrees where $\theta_{O3}$ and $\theta_{O1}$ are phase angles of $i_{O3}$ and $i_{O1}$, respectively) yields the oscillation frequency $\omega_0$

$$\omega_0 = \frac{1}{\tau_b \sqrt{\left(A_0 \frac{\tau_a}{\tau_b}\right)}} \tag{14}$$

Analytic treatments for the results shown in (14) have been provided in Adisorn Leelasantitham (2007). On the other hand, it follows from (13) that $\varnothing_b = \angle F_2(s) + \angle F_3(s) = -90^o$ (i.e. $F_2(s) \cdot F_3(s) = i_{O3} / i_{O1}$ provides a quadrature phase shift of $\varnothing_b = \theta_{O3} - \theta_{O1} = -90$ degrees) yields the oscillation frequency $\omega_0$

$$\boldsymbol{\omega}_0 = \frac{1}{\boldsymbol{\tau}_b} \sqrt{\frac{\boldsymbol{\tau}_b}{\left[\boldsymbol{\tau}_c \left(1 + \frac{\boldsymbol{\tau}'_a}{\boldsymbol{\tau}_b}\right) + \boldsymbol{\tau}'_a\right]}} \tag{15}$$

Analytic treatments for the results shown in (15) have been provided in Adisorn Leelasantitham (2007). As a result, therefore, (14) = (15) and $A_0$ is equal to

$$A_0 = \frac{\boldsymbol{\tau}_c}{\boldsymbol{\tau}_a} + \left(\frac{\boldsymbol{\tau}'_a \boldsymbol{\tau}_c}{\boldsymbol{\tau}_b \boldsymbol{\tau}_a}\right) + \frac{\boldsymbol{\tau}'_a}{\boldsymbol{\tau}_a} \tag{16}$$

As mentioned earlier in Section IIB, $\tau_a = C_a/g_{m1}$ and $\tau_b = C_b/g_{m3}$, substituting $\tau_a$ and $\tau_b$ in (14) with ($\tau_a = C_a/g_{m1}$) and ($\tau_b = C_b/g_{m3}$) yields $\omega_0 = (g_{m3}/C_b) / [A_0(C_a/g_{m1})(g_{m3}/C_b)]^{-1/2}$, as will be seen later in Section IIIB, $g_{m1} = g_{m3}$, and therefore

$$\omega_0 = \frac{2I}{\left[\sqrt{\left(A_0 \frac{C_a}{C_b}\right)}\right](V_{GS3} - V_T)C_b} \tag{17}$$

It can be seen from (17) that $\omega_0$ is tunable through the bias current I. Such an oscillator employs a low-pass-filter-based current-mirror technique based on (i) inherent time constants of current mirrors as described in (14) or (17), i.e. the internal capacitances and the transconductance of a diode-connected NMOS and (ii) a simple negative resistance $R_N$ formed by a resistor load $R_L$ of a current mirror as described in (7).

## III. An Example of Detailed Analysis

### A. Internal Capacitances of CMOS Current Mirrors

Theoretically, two basic types of internal capacitances of a MOS transistor $Q_i$ are the gate capacitive effects and the junction capacitances (Sedra and Smith, 1998). The gate capacitive effects are modeled by three capacitances $C_{gsi}$, $C_{gdi}$ and $C_{gbi}$, whilst the junction capacitances are modeled by two capacitances $C_{dbi}$ and $C_{sbi}$ (Sedra and Smith, 1998). The subscripts g, s, d, b and i refer to the gate, source, drain, body and $Q_i$, respectively. A total intrinsic gate capacitance (Christian and Cheng, 2000) $C_{Gi}$ is the summation of the three gate capacitive effects, i.e. $C_{Gi} = C_{gsi} + C_{gdi} + C_{gbi}$.

Practically, effects of additional parasitic capacitances from, for example, metal tracks or other environments may be included and therefore degradation of performance may be expected. For purposes of simplicity, a particular example in this section demonstrates use of internal capacitances of current mirrors where effects of other parasitic capacitances have not been considered.

As a particular example of the low-pass-filter-based technique, transistors are modeled by Alcatel Mietec 0.5 μm CMOS C05MD Technology (AMC) of EUROPRACTICE. The minimum width W and length L of a transistor are 0.8 μm and 0.5 μm, respectively. In this technique, Table 2(a) shows internal capacitances $C_{gsi}$, $C_{gdi}$, $C_{gbi}$, $C_{dbi}$, $C_{sbi}$ and the total intrinsic gate capacitance $C_{Gi}$ of individual MOS transistors $Q_i$, of Fig. 2 for i = 1 to 18, using aspect ratios W/L, 2W/L or $G_0$(W/L). In addition, Table 2(b) describes internal capacitances $C_a$, $C_b$, $C_a'$, $C_b'$ and $C_c$ at nodes N, P, N′, P′ and T, respectively, of individual CMOS current mirrors in Fig. 2.

**Table 2** Internal capacitances of (a) MOS transistors and (b) CMOS current mirrors

| Aspect ratios | | | W/L | | | $G_0$(W/L) | | 2W/L |
|---|---|---|---|---|---|---|---|---|
| Transistors | | | NMOS | | PMOS | NMOS | PMOS | PMOS |
| | | | $Q_1$, $Q_3$, $Q_5$, $Q_7$, $Q_9$ | $Q_2$, $Q_6$ | $Q_{11}$, $Q_{12}$, $Q_{15}$, $Q_{18}$ | $Q_4$, $Q_8$, $Q_{10}$ | $Q_{14}$, $Q_{17}$ | $Q_{13}$, $Q_{16}$ |
| $g_{mi}$ ($\times 10^{-4}\ \Omega^{-1}$) | | | 1.0638 | 1.0638 | 0.4167 | $G_0$ (1.0638) | $G_0$ (0.4167) | 0.8333 |
| Capacitances of ($\times 10^{-15}$ F) | (a) transistors | $C_{gsi}$ | 1.6 | 1.6 | 1.6 | $G_0$ (1.6) | $G_0$ (1.6) | 3.2 |
| | | $C_{gdi}$ | Short | 0.16 | 0.16 | $G_0$ (0.16) | $G_0$ (0.16) | 0.32 |
| | | $C_{gbi}$ | 0.48 | 0.48 | 0.48 | $G_0$ (0.48) | $G_0$ (0.48) | 0.96 |
| | | $C_{dbi}$ | 0.16 | 0.16 | 0.16 | $G_0$ (0.16) | $G_0$ (0.16) | 0.32 |
| | | $C_{sbi}$ | Short | Short | Short | Short | Short | Short |
| | | $C_{Gi}$ | 2.08 | 2.24 | 2.24 | $G_0$ (2.24) | $G_0$ (2.24) | 4.48 |
| | (b) current mirrors | $C_a$ | $C_{G1} + C_{G2} + C_{db1} + C_{db10} + C_{db12}$ = 4.64 + $G_0$ (0.16) | | | | | |
| | | $C_b$ | $C_{G3} + C_{G4} + C_{db3} + C_{db2} + C_{db13}$ = 2.72 + $G_0$ (2.24) | | | | | |
| | | $C_a'$ | $C_{G5} + C_{G6} + C_{db5} + C_{db4} + C_{db14} + C_{db15}$ = 4.64 + $G_0$ (0.32) | | | | | |
| | | $C_b'$ | $C_{G7} + C_{G8} + C_{db7} + C_{db6} + C_{db16}$ = 2.72 + $G_0$ (2.24) | | | | | |
| | | $C_c$ | $C_{G9} + C_{G10} + C_{db9} + C_{db8} + C_{db17} + C_{db18}$ = 2.40 + $G_0$ (2.56) | | | | | |

**B. Internal Time Constants $\tau_a$, $\tau_b$, $\tau'_a$, $\tau'_b$, $\tau_c$ and $\tau_d$**

Transconductances $g_{mi}$ of individual transistors $Q_i$ are also summarized in Table 2 at I = 20 μA. For NMOS transistors, $V_{GSi}$ = 1.056 V for i = 1 to 10, $V_T$ = 0.68 V (maximum $V_T$ = 0.71 V, typical $V_T$ = 0.61 V and minimum $V_T$ = 0.51 V). For PMOS transistors, $|V_{GSi}|$ = 1.64 V for i = 11 to 18, $V_T$ = –0.68 V (maximum $V_T$ = –0.49 V, typical $V_T$ = –0.59 V and minimum $V_T$ = –0.68 V). By using Table 2, the internal time constants $\tau_a$, $\tau_b$, $\tau'_a$, $\tau'_b$, $\tau_c$ and $\tau_d$ previously described in Section IIB can be summarized in terms of $G_0$, as shown in Table 3(a). It can be seen from Tables 2 and 3(a) that $g_{m3} = g_{m7}$, $C_b = C_b'$ and therefore $\tau_b = \tau'_b$.

**Table 3** Time constants, (a) in terms of $G_0$ or $A_0$, (b) calculated from the analysis (c) calculated for the simulation

| | Time constants | | | |
|---|---|---|---|---|
| | (sec) | (a) ($\times 10^{-11}$ sec) | (b)Analysis<br>$G_0 = 1.0429$, $A_0 = 3.1269$<br>($\times 10^{-11}$ sec) | (c) Simulation<br>$G_0 = 1.1$, $A_0 = 3.1626$<br>($\times 10^{-11}$ sec) |
| $\tau_a$ | $C_a/g_{m1}$ | $4.36172 + G_0(0.15040)$ | 4.51857 | 4.52716 |
| $\tau_b$ | $C_b/g_{m3}$ | $2.55687 + G_0(2.10566)$ | 4.75286 | 4.87310 |
| $\tau'_a$ | $C_a'/g_{m5}$ | $4.36172 + G_0(0.30081)$ | 4.67544 | 4.69261 |
| $\tau'_b$ | $C_b'/g_{m7}$ | $2.55687 + G_0(2.10566)$ | 4.75286 | 4.87310 |
| $\tau_c$ | $C_c/g_{m9}$ | $2.25606 + G_0(2.40647)$ | 4.76577 | 4.90318 |
| $\tau_d$ | $A_0\tau_a = A_0(C_a/g_{m1})$ | $A_0[4.36172 + G_0(0.15040)]$ | 14.12912 | 14.31760 |

**C. Resulting Sinusoidal Quadrature Oscillation**

The value of $G_0$ can be found by the following four steps. Firstly, substituting $\tau_a$, $\tau_b$, $\tau'_a$ and $\tau_c$ in (16) with those in Table 3(a) yields $A_0$ in terms of $G_0$, i.e. $A_0 = f(G_0)$. Secondly, substituting $\omega_0$ in (12) with (14) yields $G_0$ in terms of $\tau_a$, $\tau_b$, $\tau'_a$, $\tau_c$, $\tau_d$ and $A_0$, i.e. $G_0 = f(\tau_a, \tau_b, \tau'_a, \tau_c, \tau_d, A_0)$. Thirdly, substituting $\tau_a$, $\tau_b$, $\tau'_a$, $\tau_c$, $\tau_d$ of the resulting $G_0$ found in the second step with those in Table 3(a) yields $G_0$ in terms of the only $A_0$, i.e. $G_0 = f(A_0)$. Finally, substituting $A_0$ of the resulting $G_0$ found in the third step with $A_0$ found in the first step yields the only unknown $G_0$ in (12). As a result, the unknown $G_0$ can be solved and therefore

$$G_0 = 1.0429 \tag{18}$$

The value of $A_0$ can be found by the following two steps. Firstly, substituting $G_0$ in Table 3(a) with (18) yields the values of $\tau_a$, $\tau_b$, $\tau'_a$, $\tau'_b$ and $\tau_c$,' as summarized in Table 3(b) in the column analysis. Secondly, substituting $\tau_a$, $\tau_b$, $\tau'_a$, and $\tau_c$ in (16) with those in Table 3(b) yields

$$A_0 = 3.1269 \tag{19}$$

The value of time constant $\tau_d$ can be found by substituting $G_0$ and $A_0$ in Table 3 (a) with (18) and (19), respectively. As a result, values of all time constants $\tau_a$, $\tau_b$, $\tau'_a$,$\tau'_b$, $\tau_c$ and $\tau_d$ can be summarized in Table 3(b). The value of $R_N$ can be found by substituting $A_0$ in (10) with (19) and $g_{m1}$ in (10) with that shown in Table II, i.e. $g_{m1}$ = $1.0638 \times 10^{-4}\Omega^{-1}$. As a result, $R_N = -13.82$ k$\Omega$. Following (7) yields

$$R_N = 13.82 \text{ k}\Omega. \tag{20}$$

The value of the oscillation frequency $\omega_0$ can be found by the following two steps. Firstly, substituting $G_0$ in Table 2 with (18) yields the values of $C_a = 4.8069\times10^{-15}$ F and $C_b = 5.0561\times10^{-15}$ F. Secondly, substituting $g_{m3}$, $C_a$, $C_b$ in (17) with those shown in Table 2, i.e. $g_{m3} = (2I) / (V_{GS3}-V_T) = 1.0638 \times 10^{-4}\ \Omega^{-1}$, $C_a = 4.8069 \times 10^{-15}$ F, $C_b = 5.0561 \times 10^{-15}$ F and substituting $A_0$ in (17) with (19) yields $\omega_0 = 12.18 \times 10^9$ rad/s at I = 20 $\mu$A. Therefore the oscillation frequency $f_0$ = $\omega 0/2\pi$ is

$$f_0 = 1.94 \text{ GHz} \tag{21}$$

By using (18) and Table 3(b), the values of the magnitudes and the phase shift of $F_1(s)$, $F_2(s)$, $F_3(s)$, $F_4(s)$ and L(s) can be summarized in Table 4(a) in the columns analysis. It can be seen from Table 4(a) that the magnitudes and the phase shift of the loop gain L(s) typically fulfill the oscillation criteria at 1.0 and 0 degrees, respectively. It follows from Table 4(a) that $F_2(s) \cdot F_3(s)$ = $i_{O3} / i_{O1}$ provides a quadrature phase shift of $\theta_{O3} - \theta_{O1} = -90$ degrees where $\theta_{O3}$ and $\theta_{O1}$ are phase angles of $i_{O3}$ and $i_{O1}$, respectively. In other words, $i_{O3}$ and $i_{O1}$ provide quadrature oscillation, i.e. $i_{O3} = K_0\sin\theta_{O3}$ and $i_{O1} = K_0\sin\theta_{O1} = K_0\sin(\theta_{O3}+90) = K_0\cos\theta_{O3}$ where $K_0$ represents an appropriate amplitude. For these reasons, the circuit in Fig. 2 is a sinusoidal quadrature oscillator.

**Table 4** Magnitudes and phase angles of current gains $F_1(s)$, $F_2(s)$, $F_3(s)$, $F_4(s)$ and loop gain $L(s)$ of Fig. 2, (a) calculated from the analysis, (b) calculated for the simulation

| Gains | | Magnitudes | | Phase angles (Degrees) | | | | |
|---|---|---|---|---|---|---|---|---|
| | | (a) Analysis | (b) Simulation | Phase shift | (a) Analysis | | (b) Simulation | |
| | | $G_0 = 1.0429$ | $G_0 = 1.100$ | | $G_0 = 1.0429$ | | $G_0 = 1.100$ | |
| $F_4(s)$ | -1 | 1 | 1 | $\angle -1$ | | 180° | | 180° |
| | $F_5(s)$ | 1.792 | 1.81 | $\tan^{-1}\omega_0\tau_a$ | 29° | -90° | -28.5° | -90° |
| | | | | $-\tan^{-1}\omega_0\tau_d$ | -60° | | -59.7° | |
| $F_1(s)$ | | 0.790 | 0.84 | $-\tan^{-1}\omega_0\tau_a$ | -29° | | -28.5° | |
| | | | | $-\tan^{-1}\omega_0\tau_b$ | -30° | | -30.3° | |
| $F_2(s)$ | | 0.784 | 0.83 | $-\tan^{-1}\omega_0\tau'_a$ | -30° | -90° | -29.3° | -90° |
| | | | | $-\tan^{-1}\omega_0\tau'_b$ | -30° | | -30.3° | |
| $F_3(s)$ | | 0.902 | 0.95 | $-\tan^{-1}\omega_0\tau_c$ | -30° | | -30.4° | |
| $L(s)$ | | 1.001 | 1.20 | $\angle L(s)$ | | 0° | | 0° |

### D. Ratio of Oscillation Frequency to Unity-Gain Frequency

The total intrinsic gate capacitances $C_{Gi}$ determines the unity current-gain frequency $\omega_{Ti}$ (Baker, Li and Boyce, 1998) or the unity-gain frequency $f_{Ti} = \omega_{Ti} / (2\pi)$ (Sedra and Smith, 1998) of $Q_i$. Typically (Baker, Li and Boyce, 1998),

$$\omega_{Ti} = \frac{1}{\tau_i} \tag{22}$$

where $\tau_i = C_{Gi} / g_{mi}$. It can be seen from Table 2 that, for a minimum aspect ratio W/L, $C_{Gi}$ and $g_{mi}$ of an NMOS $Q_i$ are $2.2400\times 10^{-15}$ F and $1.0638 \times 10^{-4}\Omega^{-1}$, respectively. Therefore, the unity-gain frequency ($f_T$) of an NMOS $Q_i$ in this particular example is approximately $f_{Ti}$ = 7.56 GHz. The ratio of the oscillation frequency $\omega_0$ (17) to the unity current-gain frequency $\omega_{Ti}$ (22) yields

$$\frac{\omega_0}{\omega_{Ti}} = \left[\frac{g_{m3}/C_b}{\sqrt{\left(A_0\dfrac{C_a}{C_b}\right)}}\right]\left(\frac{C_{Gi}}{g_{mi}}\right) \tag{23}$$

Consequently,

$$\frac{f_0}{f_{Ti}} = 0.257 \tag{24}$$

## IV. Simulation Results

The performance of the circuit shown in Fig. 2 has been simulated through SPICE. As mentioned earlier, transistors are modeled by AMC. The supply voltage $V_{dd}$ = 2 V and $R_1$ = 18 k$\Omega$. For purposes of simulation, the values of $G_0$ previously found in (18) and $R_L$ previously found in (20) are practically chosen to be 1.1 and 14 k$\Omega$, respectively. By using $G_0$ = 1.1, the corresponding values of time constants $\tau_a$, $\tau_b$, $\tau'_a$, $\tau'_b$, $\tau_c$, and $\tau_d$ are summarized in Table 3(c) in the column simulation and can be directly compared to those in Table 3(b) in the column analysis.

Similarly, the corresponding values of the magnitudes and the phase shift of individual gains are summarized in Table 4(b) in the columns simulation where $G_0$ = 1.1, and can be directly compared to those in Table 4(a) in the columns analysis. It should be noted from Table 4(b) that the magnitude of the loop gain L(s) = 1.20 for the simulation, and is more than unity as a result from a sufficiently large value of the gain factor $G_0$ associated with the aspect ratio W/L (see Table 2). Such gains sufficiently initiate and practically sustain the oscillation. Table 5 compares resulting values of various parameters between the analysis and the simulation of Fig. 2.

**Table 5** Values of parameters for sinusoidal quadrature oscillation of Fig. 2

| | Equations | Analysis | Simulation |
|---|---|---|---|
| $G_0$ | Eqn (18) | 1.0429 | 1.1000 |
| $A_0$ | Eqn (19) | 3.1269 | 3.1626 |
| $\omega_0$ | Eqn (17) | 12.18 Grad/s | 11.97 Grad/s |
| $f_0$ | $\omega_0/2\pi$ | 1.94 GHz | 1.90 GHz |
| $R_N$ | Eqn (10) | –13.82 k$\Omega$ | –14 k$\Omega$ |
| $R_L$ | Eqn (20) | 13.82 k$\Omega$ | 14 k$\Omega$ |
| $\omega_0/\omega_{Ti}$ | Eqn (23) | 0.257 | 0.25 |

Figure 3 depicts the resulting cosine and sine oscillograms of the quadrature currents $i_{O1}$ and $i_{O3}$, respectively, at I = 20 $\mu$A, where the oscillation frequency $f_0 = \omega_0/(2\pi)$ is measured as 1.9 GHz. Figure 4 illustrates plots of the oscillation frequencies (GHz) and the amplitudes (dB) of $i_{O1}$ versus bias current I, where the dotted lines indicate the expected analysis and the solid lines indicate the SPICE analysis. As shown in Fig. 4, the oscillation frequencies are tunable over a range from 1.53 to 1.9 GHz by the bias current I from 13 to 20 uA, respectively, and therefore the tuning range is approximately 370 MHz or 21.6%.

Figure 5 depicts the amplitude matching (dB) in terms of the ratio $i_{O3}$ / $i_{O1}$ as well as the quadrature phase matching (degrees) in terms of ($\theta_{O3}-\theta_{O1}$) of the quadrature currents versus frequency. The amplitude matching is as near as 0.029 dB, whilst the quadrature phase matching for

$-90^{\circ}$ is better than $0.15^{\circ}$. Figure 6 shows the power spectrum levels (dBm) of the fundamental frequency at 1.9 GHz and the next harmonics of the oscillogram $i_{O1}$ previously depicted in Fig. 3 using a commercially available fast Fourier transform (FFT) program. As shown in Fig. 6, the distortions are due mainly to the presence of the second harmonics, which is approximately 51.5 dB down from the fundamental frequency, and they remain essentially at the same magnitude over the entire operational bias-current range (13 μA to 20 μA). Consequently, the total harmonic distortions (THD) are less than 0.3%.

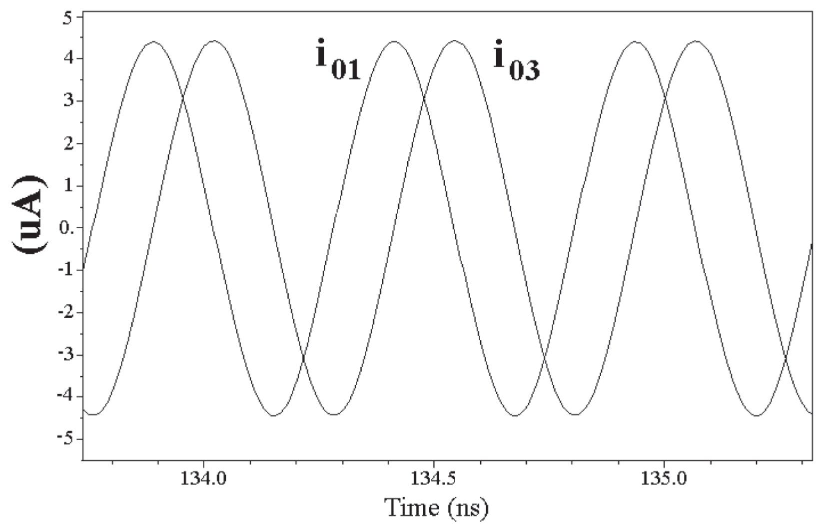


**Fig. 3** Oscillograms of quadrature currents $i_{O1}$ and $i_{O3}$ at 1.9 GHz and I = 20 μA

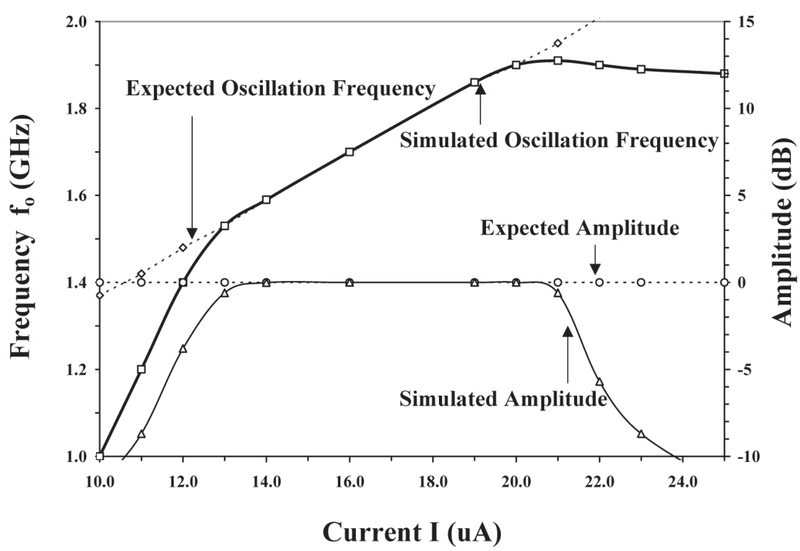


**Fig. 4** Plots of the oscillation frequencies and the amplitude of $i_{O1}$ versus bias current I

As shown in Fig. 6, the phase noise is equal to –90.01 [dBc/Hz] at 2 MHz offset from the 1.9 GHz carrier. In other words, CNR = 90.01 dBc/Hz at $\Delta f$ = 2 MHz and $f_0$ = 1.9 GHz. It can be seen from Fig. 2 that the total current consumption of the oscillator is equal to $8I + 3G_0I$. For $I = 20\ \mu A$ and $G_0 = 1.1$, the power dissipation ($P_{DC}$) is only 0.452 mW. Consequently, the figure of merit (Sansen, Huijsing, and Van De Plassche, eds., 1999) called $CNR_{norm}$ = 153.03 dBc/Hz.

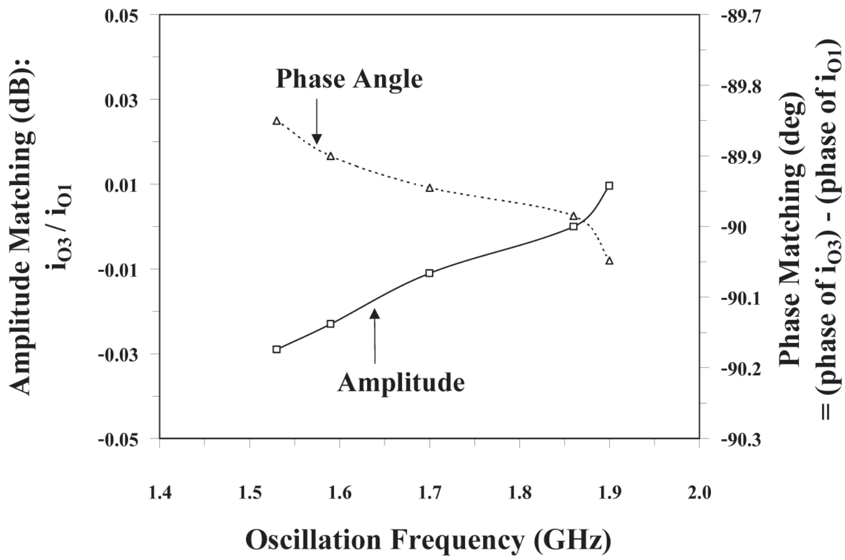


**Fig. 5** Amplitude and phase matching of the quadrature signals versus frequency

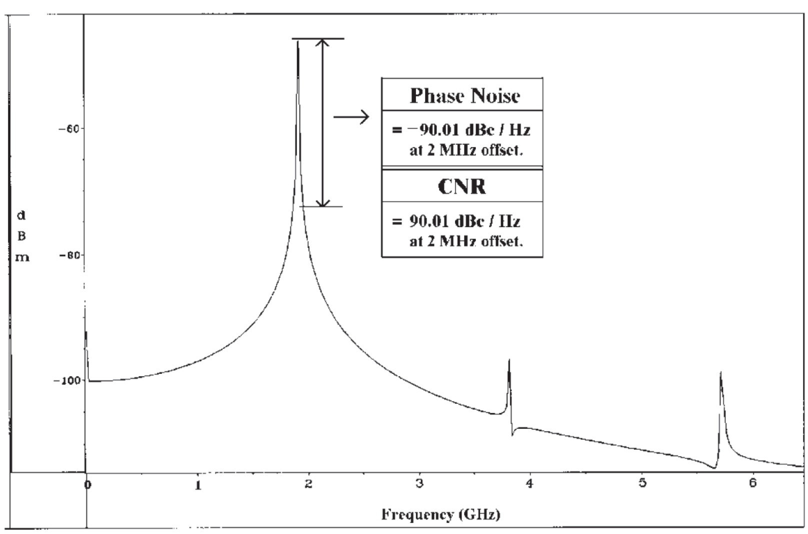


**Fig. 6** Harmonic spectrums through FFT of the oscillogram $i_{O1}$ previously depicted in Fig. 3 and carrier-to-noise ratio (CNR) = 90.01 dBc/Hz at 2 MHz offset from the 1.9 GHz carrier

## V. Comparisons to Other Techniques (Under the Conditions of the Tuning Ranges of the Oscillation Frequencies from 1.805 to 1.99 GHz)

As mentioned earlier in Section I, the required operating frequencies between 1.805 to 1.99 GHz in the receivers are typically utilized in GSM 1800 MHz or PCS 1.9 GHz. In the well publicized literature, no other RC linear QOs have been reported for the tuning ranges of the high oscillation frequencies from 1.805 to 1.99 GHz; therefore, existing RC techniques for QOs have been excluded from Table 6.

For the sake of completeness (under the conditions of the tuning ranges of the oscillation frequencies from 1.805 to 1.99 GHz), irrelevant simulation or experimental results of the LC (Andreani, 2002; Kao and Wu, 2000; Razavi, 1997b) and the non-linear (Anand and Razavi, 2001; Bautista and Aranda, 2004; Finocchiaro, et al., 1999; Van Der Tang and Kasperkovitz, 1997) QOs may be included in Tables 6(a) and (b), although comparisons are somewhat unfair in terms of their different categories from RC linear QOs.

It can be seen from Table 6 that this paper offers not only the power consumption of 0.45 mW compared to others between 7.05 to 100 mW, but also the $f_0/f_T$ of 0.25 compared to others between 0.1 to 0.2. In addition, the total harmonic distortion (THD) in this paper is also improved. By using better transistors with very much higher $f_T$ or more than 7.56 GHz, much higher and more useful oscillation frequencies can be expected as suggested in (23). This work therefore offers not only much better performance compared to other RC techniques, but also a potential alternative to a low-power high-frequency sinusoidal quadrature oscillator.

**Table 6** Performances of the proposed techniques compared to those of other (a) LC techniques and (b) ring techniques. (Under the conditions of the tuning ranges of the oscillation frequencies from 1.805 to 1.99 GHz)

| | References | | Linear quadrature oscillators | | | | Non-linear quadrature oscillators | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | RC techniques | (a) LC techniques | | | (b) Ring techniques | | | |
| | | | CMOS | CMOS | | | CMOS | | BJTs | |
| | Performances | | PROPOSED CIRCUIT | Razavi (1997b). | Kao and Wu (2000). | Andreani (2002). | Anand and Razavi (2001). | Bautista and Aranda (2004). | Tang and Kasperkovitz (1997). | Finocchiaro et al. (1999). |
| Performances | $f_o$ | GHz | 1.9 | 1.8 | 1.95 | 1.97 | 2.5 | 2.1 | 2.2 | 1.8 |
| | $f_T$ | GHz | 7.56 | - | - | - | - | - | 11 | 18 |
| | $f_o / f_T$ | - | 0.25 | - | - | - | - | - | 0.2 | 0.1 |
| | TR | GHz | 0.37 | 0.12 | 0.27 | 0.33 | 0.8 | 1.9 | 1.3 | 1 |
| | $P_{DC}$ | mW | 0.45 | 15 | 19 | 50 | 10 | 7.01 | 100 | 22.5 |
| | AM | dB | < 0.029 | - | < 0.001 | - | - | - | < 0.1 | - |
| | QPM | deg | < 0.15° | - | < 1 | < 0.25 | - | - | < 0.5 | - |
| | THD | % | < 0.3 | - | - | - | - | - | - | - |
| | $CNR_{norm}$ | dBc/Hz | 153.03 | - | - | - | - | - | 146.8 | 153.5 |
| Using | (1) All Current Mirrors | | √ | × | - | × | × | × | × | × |
| | (2) Internal Capacitances | | √ | × | - | × | √ | √ | √ | √ |
| | (3) Small-Signal Resistance ($1/g_m$) | | √ | × | × | × | √ | √ | √ | √ |
| | (4) Negative Resistance | | √ | × | × | × | × | × | × | × |
| Simulation results | | | √ | √ | √ | √ | √ | × | √ | √ |
| Experimental results | | | × | √ | × | √ | √ | √ | √ | × |

*Note* that $f_0$ = oscillation frequency, $f_T$ = unity-gain frequency, $f_0/f_T$ = ratio of $f_0/f_T$, tuning range (TR), $P_{DC}$ = power consumption, AM = amplitude matching, QPM = quadrature phase matching, THD = total harmonic distortion, $CNR_{norm}$ = normalized carrier-to-noise ratio, √ = Yes, × = No.

## VI. Discussion

Effects of variations in components $C_a$, $C_b$, $C'_a$, $C'_b$, $C_c$ and $R_L$ may result in other on time constants $\tau_a$, $\tau_b$, $\tau'_a$, $\tau'_b$, $\tau_c$, and $\tau_d$. In particular, the oscillation frequency may be increased (or decreased) due to the increases (or decreases) in the values of $C_a$, $C_b$, $C'_a$, $C'_b$, $C_c$ and $R_L$. In addition, the variations of temperature (T) may result in other on transconductances $g_{m1}$, $g_{m3}$, $g_{m5}$, $g_{m7}$ and $g_{m9}$. For example, the increased (or decreased) temperature may be decreased (or increased) in the values of the transconductances [$g_m = (2I) / (V_{GS}-V_T)$], i.e.

if T↑, then $V_{GS}$↑, $V_T$↓ and I↑, where ↑ is an increase and ↓ is a decrease. Therefore, the oscillation frequency may be decreased (or increased), as shown in (17), due to the increases (or decreases) in the values of temperature.

Figure 7 depicts the oscillation frequency $f_0$ (GHz) versus percents of the variations of components ($C_a$, $C_b$, $C_a'$, $C_b'$, $C_c$ and $R_L$) as well as the variations of temperature (°C). The dotted and solid lines indicate the resulting oscillation frequencies for the variations of components and temperature, respectively. As shown in Fig. 7, the dotted line in the case of the variations of components between -1.5% and 1.5% indicates that the oscillation frequency is varied in the range between 1.8 GHz to 1.9 GHz, whilst the solid line in the case of the variations of temperature between 20 °C and 100 °C indicates that the oscillation frequency is reduced from 1.9 GHz to 1.7 GHz.

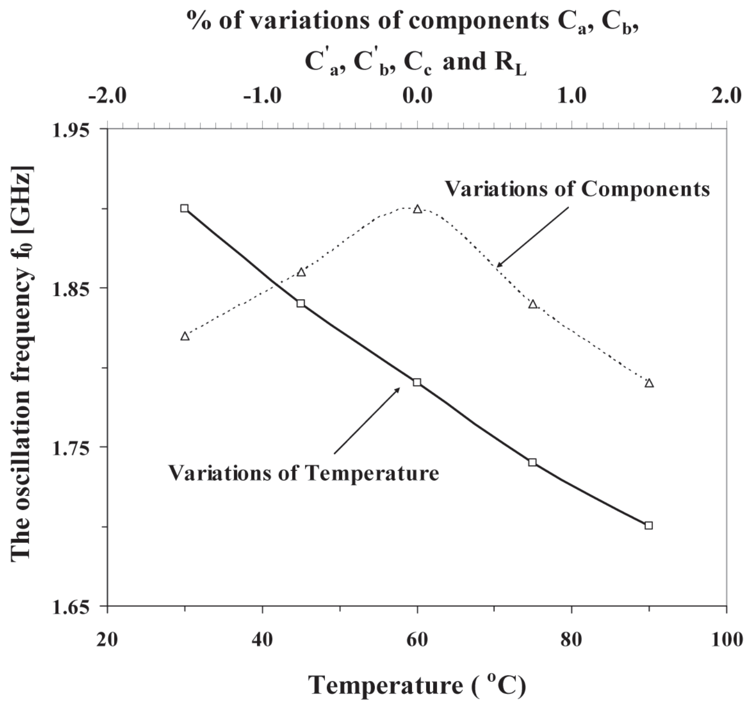


**Fig. 7** The oscillation frequency versus percents of the variations of components ($C_a$, $C_b$, $C_a'$, $C_b'$, $C_c$ and $R_L$) as well as the variations of temperature

## VII. Conclusions

The Design and analysis of the low-power high-frequency CMOS sinusoidal quadrature oscillator has been presented through the use of two $2^{nd}$-order low-pass current mirror (CM)-based filters ($F_1$ and $F_2$), a $1^{st}$-order CM low-pass filter ($F_3$) and a CM bilinear transfer function ($F_4$). The bilinear transfer function ($F_4$) is described in terms of a negative resistance ($R_N = -R_L$), where $R_L$ is the resistor load of a current mirror. The technique is relatively simple based on (i) inherent time constants of current mirrors, i.e. the internal capacitances and the transconductance of a diode-connected NMOS, and (ii) a simple negative resistance $R_N$ formed by a load resistor $R_L$ of a current mirror. Neither external capacitances nor inductances are required. The oscillation frequency ($f_0$) is 1.9 GHz and is current-tunable over a range of 370 MHz or 21.6%. The power consumption is at approximately 0.45 mW. The amplitude matching and the quadrature phase matching are better than 0.05 dB and 0.15$^{o}$, respectively. Total harmonic distortions (THD) are less than 0.3%. At 2 MHz offset from the 1.9 GHz, the carrier to noise ratio (CNR) is 90.01 dBc/Hz, whilst the figure of merit called a normalized carrier-to-noise ratio ($CNR_{norm}$) is 153.03 dBc/Hz. The ratio of the oscillation frequency ($f_0$) to the unity-gain frequency ($f_T$) of a transistor is 0.25. The variations of components between -1.5% and 1.5% has indicated that the oscillation frequency is varied in the range between 1.8 GHz to 1.9 GHz, whilst the variations of temperature between 20 $^{o}$C and 100 $^{o}$C has indicated that the oscillation frequency is reduced from 1.9 GHz to 1.7 GHz. Comparisons to other approaches have also been included.

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## References

Adisorn Leelasantitham. 2007. “Analysis of a High-Frequency Low-Power CMOS Low-Pass-Filter-Based Current-Mirror Sinusoidal Quadrature Oscillator.” **University of the Thai Chamber of Commerce Journal** 27, 3: 305-323.

Adisorn Leelasantitham, and Banlue Srisuchinwong. 2003. “A High-Frequency Low-Power Sinusoidal Quadrature Oscillator Using Only CMOS Current Mirrors.” In **The 15th International Conference on**

**Microelectronics (ICM03),** pp. 404-408. Cairo: IEEE.

_______. 2004a. "A High-Frequency Low-Power All-NMOS All-Current-Mirror Sinusoidal Quadrature Oscillator." In **The 2004 IEEE Region 10 Conference (TENCON 2004),** pp. 364-367. Chiang Mai: IEEE.

_______. 2004b. "A Low-Power, High-Frequency, All-NMOS All-Current-Mirror Sinusoidal Quadrature Oscillator." **Microelectronics Journal** 35: 713-721.

_______. 2004c. "A Low-Power High-Frequency CMOS Current-Mirror Sinusoidal Quadrature Oscillator." **IEICE TRANSACTIONS on Fundamentals of Electronics, Communications and Computer Sciences E87-A,** 11: 2964-2972.

_______. 2007. "A High-Frequency Low-Power Low-Pass-Filter-Based All-Current-Mirror Sinusoidal Quadrature Oscillator." **International Journal of Applied Science, Engineering and Technology** 3, 1: 18-23.

_______. 2009. "A Low-Power High-Frequency All-Pass-Filter-Based Sinusoidal Quadrature Oscillator Using CMOS Current Mirrors." In **The 2008 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS 2008),** pp. 159-163. Bangkok: IEEE.

Anand, S.B., and B. Razavi. 2001. "A CMOS Clock Recovery Circuit for 2.5-Gb/s NRZ Data." **IEEE Journal of Solid-State Circuits** 36, 3: 432-439.

Andreani, P. 2002. "A Low-Phase-Noise Low-Phase-Error 1.8GHz Quadrature CMOS VCO." In **Proceedings of the 2002 IEEE International Solid-State Circuits Conference,** pp. 228-229. San Francisco: IEEE.

Baker, R.J., Li, H.W., and Boyce, D.E. 1998. "CMOS Circuit Design, Layout and Simulation." **IEEE Press:** 174.

Banlue Srisuchinwong. 2000. "Fully Balanced Current-Tunable Sinusoidal Quadrature Oscillator." **International Journal of Electronics** 87: 547-556.

Bautista, D.P., and Aranda, M.L. 2004. "A Low Power and High Speed CMOS Voltage-Controlled Ring Oscillator." In **Proceeding of the 2004 IEEE International Symposium on Circuits and Systems,** pp. 752-755. Vancouver: IEEE.

Cakir, C., Cam, U., and Cicekoglu, O. 2005. "Novel Allpass Filter Configuration Employing Single OTRA." **IEEE Transaction on Circuits and System-II: Express Briefs** 52, 3: 122-125.

Christian, Enz., and Cheng, Y. 2000. "MOS Transistor Modeling for RF IC Design." **IEEE Journal of Solid-State Circuits** 35: 188.

Fenk, J. 1997. "Highly Integrated RF-IC's for GSM and DECT Systems-A Status Review." **IEEE Transaction on Microwave Theory and Techniques** 45, 12: 2531-2539.

Finocchiaro, S., et al. 1999. "Design of Bipolar RF Ring Oscillators." In **Proceedings of the 6th IEEE International Conference on Electronics, Circuits and Systems (ICECS'99),** pp. 5-8. Pafos: IEEE.

Gatta, F., et al. 2004. "A Fully Integrated 0.18-μm CMOS Direct Conversion Receiver Front-End with On-Chip LO for UMTS." **IEEE Journal of Solid-State Circuits** 39, 1: 15-23.

Horng, J.W., Chou, H.P., and Shiu, I.C. 2006. "Current-Mode and Voltage-Mode Quadrature Oscillator Employing Multiple Outputs CCIIs and Grounded Capacitors." In **Proceeding of the 2006 IEEE International Symposium on Circuits and Systems,** pp. 4. Kos: IEEE.

Hughes, J.B., et al. 2002. "1 mW CMOS Polyphase Channel Filter for Bluetooth." **IEE Proc.-Circuits Devices Syst.** 149, 5/6: 348-354.

Johns, D.A., and Martin, K. 1997. **Analog Integrated Circuit Design.** New York: Wiley.

Kao, H.-S., and Wu, C.-Y. 2000. "A Compact CMOS 2V Low-Power Direct-Conversion Quadrature Modulator Merge with Quadrature Voltage-Controlled Oscillator and RF Amplifier for 1.9GHz RF Transmitter Applications." In **Proceedings of the 2000 IEEE International Symposium on Circuits and Systems,** pp. 765-768. Geneva: IEEE.

Kiattisak Kumwachara, and Wanlop Surakampontorn. 2003. "An Integrable Temperature-Insensitive $g_m$-RC Quadrature Oscillator." **International Journal of Electronics** 90, 9: 599-605.

Parssinen, A. 2001. **Direct Conversion Receivers in Wide-Band Systems.** Dordrecht: Klumer Academic.

Razavi, B. 1997a. "Design Considerations for Direct-Conversion Receivers." **IEEE Transaction on Circuits and System-II** 44: 428-435.

_______. 1997b. "A 1.8 GHz CMOS Voltage-Controlled Oscillator." In **Proceedings of the 1997 IEEE International Solid-State Circuits Conference,** pp. 388-389. San Francisco: IEEE.

Sansen, W., Huijsing, J.H., and Van De Plassche, R.J., (eds.). 1999. **Analog Circuit Design.** Dordrecht: Klumer Academic.

Sedra, A., and Smith, K.C. 1998. **Micro-electronic Circuits.** 4th ed. New York: Oxford University Press.

Sitthichai Pookaiyaudom, and Jirayuth Mahattanakul. 1995. "A 3.3 Volt High-Frequency Capacitorless Electronically-Tunable Log-Domain Oscillator." In **Proceeding of the 1995 IEEE International Symposium on Circuits and Systems,** pp. 829-832. Washington: IEEE.

Sitthichai Pookaiyaudom, and Kanok Samootrut. 1987. "Current-Mirror Phase-Shifter Oscillator." **Electronics Letters** 23: 21-23.

Sitthichai Pookaiyaudom, and Rungsimant Sitdhikorn. 1996. "Current-Differencing Band-Pass Filter Realization with Application to High-Frequency Electronically Tunable Low-Supply-Voltage Current-Mirror-Only Oscillator." **IEEE Transaction on Circuits and System-II** 43,12: 832-835.

Van Der Tang, J., and Kasperkovitz, D. 1997. "A 0.9-2.2GHz Monolithic Quadrature Mixer Oscillator for Direct-Conversion Satellite Receivers." In **Proceedings of the 1997 IEEE International Solid-State Circuits Conference,** pp. 88-89. San Francisco: IEEE.

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